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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,536	11/13/2003	Ralf Brederlow	20046/0200501-US0	2199

7278 7590 01/10/2006

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EXAMINER	
RODGERS, COLLEEN E	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/714,536	BREDERLOW, RALF	
	Examiner	Art Unit	
	Colleen E. Rodgers	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/23/04 & 6/4/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: on page 10 of the instant specification, line 3, replace "105" with --106-- for consistency with previous numeral assigned to the gate portion.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 13-17 and 19-24 are rejected under 35 U.S.C. 102(b) as being anticipated by **Bao et al** (USPN 6,150,668).

4. Regarding claims 13 and 24, **Bao et al** disclose a polymer transistor arrangement and a method of forming said arrangement, comprising:

a polymer transistor formed in and/or on a substrate **205** including:

forming a first source/drain region **225**;

forming a second source/drain region **226**;

forming a channel region **230** between the first and second source/drain regions **225** and **226**;

forming a gate region **215**; and

forming a gate insulating layer **220** between the channel region **230** and the gate region **215**; and

forming a drive circuit providing the source/drain regions **225** and **226** and the gate region **215** with electrical potentials such that a junction between at least one of the source/drain regions **225** and **226** and the channel region **230** is operated as a diode [see col. 9, lines 33-34; it is inherent that when a potential is applied to a structure such as this that it will function as a diode].

Regarding claim 14, **Bao et al** disclose the arrangement of claim 13 as described above. That the drive circuit provides the source/drain region and the gate region with electrical potentials such that the junction between one of the two source/drain regions and the channel region is connected as a reverse-bias diode is merely an intended use, and therefore anticipated by **Bao et al** as the structure of **Bao et al** may be used in this manner.

Regarding claim 15, **Bao et al** disclose the arrangement of claim 13 as described above, wherein the channel region **230** and the source/drain regions **225** and **226** are produced from a material such that the junction between one of the source/drain regions **225** or **226** and the channel region **230** is a Schottky junction [see paragraph bridging cols. 6 and 7]. It is admitted in the instant specification that:

> A Schottky diode is a diode which, instead of a pn junction, uses a metal-semiconductor contact or a metal-polymer contact, the metal having a different work function that the other material that it is contact connected [see instant specification, page 4, lines 4-6].

Therefore, the structure of **Bao et al** must function in the same way.

Regarding claim 16, **Bao et al** disclose the arrangement of claim 13 as described above. As with claim 17, that the drive circuit provides electrical potentials such that the magnitude of the gate voltage is greater than the magnitude of the voltage between the source/drain regions is merely an intended use, and therefore anticipated by **Bao et al** as the structure of **Bao et al** may be used in this manner.

Regarding claim 17, **Bao et al** disclose the arrangement of claim 13 as described above, wherein the junctions between respective ones of the source/drain regions **225** and **226** are formed geometrically asymmetrically with respect to one another [see Figs. 2 and 3].

Regarding claims 19-23, **Bao et al** disclose the arrangement of claim 13 as described above. The limitations of claims 19-23 are merely intended use, and therefore are anticipated by **Bao et al** as the structure of **Bao et al** as disclosed may be used in an integrated circuit device, as a reference voltage circuit, a temperature-compensated reference voltage circuit, a current source or a voltage control circuit.

5. Claims 13-24 are rejected under 35 U.S.C. 102(e) as being anticipated by **Jackson et al** (USPN 6,720,572 B1).

Regarding claims 13 and 24, **Jackson et al** disclose a polymer transistor arrangement and a method of forming said arrangement, comprising:

a polymer transistor formed in and/or on a substrate **10** including:

forming a first source/drain region **18**;

forming a second source/drain region **24**;

forming a channel region **20, 22** between the first and second source/drain regions **18** and **24**;

forming a gate region **14**; and

forming a gate insulating layer **16** between the channel region **20, 22** and the gate region **14**; and

forming a drive circuit providing the source/drain regions **18** and **24** and the gate region **14** with electrical potentials such that a junction between at least one of the source/drain regions **18** and **24** and the channel region **20, 22** is operated as a diode [see Fig. 2; see also col. 3, lines 45-48].

Regarding claim 14, **Jackson et al** disclose the arrangement of claim 13 as described above. That the drive circuit provides the source/drain region and the gate region with electrical potentials such that the junction between one of the two source/drain regions and the channel region is connected as a reverse-bias diode is merely an intended use, and therefore anticipated by **Jackson et al** as the structure of **Jackson et al** may be used in this manner.

Regarding claim 15, **Jackson et al** disclose the arrangement of claim 13 as described above, wherein the channel region **20, 22** and the source/drain regions **18** and **24** are produced from a material such that the junction between one of the source/drain regions **18** or **24** and the channel region **20, 22** is a Schottky junction. Specifically, the channel region is formed of a material such as pentacene and 8-hydroxyquinoline aluminum (Alq) and the source/drain regions are formed from palladium and aluminum [see col. 3, lines 59-64]. It is admitted in the instant specification that:

> A Schottky diode is a diode which, instead of a pn junction, uses a metal-semiconductor contact or a metal-polymer contact, the metal having a different work function that the other material that it is contact connected [see instant specification, page 4, lines 4-6].

Therefore, the structure of **Jackson et al** must function in the same way.

Regarding claim 16, **Jackson et al** disclose the arrangement of claim 13 as described above. As with claim 17, that the drive circuit provides electrical potentials such that the magnitude of the gate voltage is greater than the magnitude of the voltage between the source/drain regions is merely

an intended use, and therefore anticipated by **Jackson et al** as the structure of **Jackson et al** may be used in this manner.

Regarding claim 17, **Jackson et al** disclose the arrangement of claim 13 as described above, wherein the junctions between the respective ones of the source/drain regions **18** and **24** and the channel region **20, 22** are formed geometrically asymmetrically with respect to one another [see Fig. 1].

Regarding claim 18, **Jackson et al** disclose the arrangement of claim 13 as described above, wherein one of the source/drain regions **24** is formed at least partially on the channel region **20, 22** and the other source/drain region **18** is formed at least partially below the channel region **20, 22** [see Fig. 1].

Regarding claims 19-23, **Tanabe** disclose the arrangement of claim 13 as described above. The limitations of claims 19-23 are merely intended use, and therefore are anticipated by **Tanabe** as the structure of **Tanabe** as disclosed may be used in an integrated circuit device, as a reference voltage circuit, a temperature-compensated reference voltage circuit, a current source or a voltage control circuit.

6. Claims 13-16 and 19-24 are rejected under 35 U.S.C. 102(e) as being anticipated by **Tanabe** (US Patent Application Publication 2004/0012018 A1).

Regarding claims 13 and 24, **Tanabe** discloses a polymer transistor arrangement and a method of forming said arrangement, comprising:

a polymer transistor formed in and/or on a substrate **10** including:

forming a first source/drain region **11**;

forming a second source/drain region **15**;

forming a channel region **13** between the first and second source/drain regions **11** and **15**;

forming a gate region **14**; and

forming a gate insulating layer **12** between the channel region **13** and the gate region **14**; and

forming a drive circuit providing the source/drain regions **11** and **15** and the gate region **14** with electrical potentials such that a junction between at least one of the source/drain regions **11** and **15** and the channel region **13** is operated as a diode [see Fig. 1; it is inherent that when a potential is applied to a structure such as this that it will function as a diode].

Regarding claim 14, **Tanabe** disclose the arrangement of claim 13 as described above. That the drive circuit provides the source/drain region and the gate region with electrical potentials such that the junction between one of the two source/drain regions and the channel region is connected as a reverse-bias diode is merely an intended use, and therefore anticipated by **Tanabe** as the structure of **Tanabe** may be used in this manner.

Regarding claim 15, **Tanabe** discloses the arrangement of claim 13 as described above, wherein the channel region **13** and the source/drain regions **11** and **15** are produced from a material such that the junction between one of the source/drain regions **11** or **15** and the channel region **13** is a Schottky junction. Specifically, the channel region is formed of a material such as pentacene [see paragraph 0016] and the source/drain regions are formed from any of various metals [see paragraphs 0022 and 0024]. It is admitted in the instant specification that:

> A Schottky diode is a diode which, instead of a pn junction, uses a metal-semiconductor contact or a metal-polymer contact, the metal having a different work function that the other material that it is contact connected [see instant specification, page 4, lines 4-6].

Therefore, the structure of **Tanabe** must function in the same way.

Regarding claim 16, **Tanabe** disclose the arrangement of claim 13 as described above. As with claim 17, that the drive circuit provides electrical potentials such that the magnitude of the gate voltage is greater than the magnitude of the voltage between the source/drain regions is merely an intended use, and therefore anticipated by **Tanabe** as the structure of **Tanabe** may be used in this manner.

Regarding claims 19-23, **Tanabe** discloses the arrangement of claim 13 as described above. The limitations of claims 19-23 are merely intended use, and therefore are anticipated by **Tanabe** as the structure of **Tanabe** as disclosed may be used in an integrated circuit device, as a reference voltage circuit, a temperature-compensated reference voltage circuit, a current source or a voltage control circuit.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. **Bai et al** (US Patent Application Publication 2004/0222412 A1), **Shtein et al** (US Patent Application Publication 2004/0191952 A1), **Tsutsui** (US Patent Application Publication 2003/0218166 A1), **Dimitrakopoulos et al** (USPN 6,981,970), **Wakita et al** (USPN 5,912,473), **Gates** (USPN 5,96,121) and **Dodabalapur** (USPN 5,596,208).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colleen E. Rodgers whose telephone number is (571) 272-8603. The examiner can normally be reached on Monday through Friday, 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CER

GEORGE ECKERT
PRIMARY EXAMINER